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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/833,953
Filing Date: April 11, 2001
Appellant(s): RACANELLI, MARCO

Racanelli, Marco
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 02/13/2006 appealing from the Office action mailed 10/04/2005.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,436,177	Zaccherini	07, 1995
5,489,547	Erdeljac et al.	02, 1996
6,156,602	Shao et al.	12, 2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-12, 14, 15 and 17-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccherini (U.S. 5,436,177) in view of Erdeljac et al. (U.S. 5,489,547) and Shao et al. (U.S. 6,156,602).

In reference to claim 1 and 14 Zaccherini (Fig.1-6) teaches an analogous method to form semiconductor device including polysilicon resistors and transistors including forming a layer (7) comprising polycrystalline silicon over a transistor gate region (4) and a field oxide region (5) on a substrate (2, 3); forming a doping barrier (10) above said polycrystalline silicon over said field oxide region (5) after forming said polycrystalline silicon layer (7); doping said layer over said transistor gate region with a first dose of a first dopant (11) after forming said doping barrier (10), wherein said first dose of said first dopant (11) is a dosage greater than required to result in said layer over said transistor gate region (4) having transistor gate electrical properties, wherein said first dopant (11) has a first conductivity type; removing said doping barrier (10) after doping said polycrystalline silicon layer (7) over said gate region (4) with said first dose

of said first dopant (11); and doping said layer over said transistor gate region (4) and said field oxide region (5) with a second dose of a second dopant (13), after said step of removing said doping barrier (10) so as to form a high resistivity resistor in said layer (7) over said field oxide region (5), wherein said second dopant (13) has a second conductivity type, wherein said first dose of said first dopant is higher than said second dose of said second dose of said second dopant, and wherein said resistor and said gate transistor region (4) are formed in a doped epitaxial layer (3), which is part of said substrate (2, 3) (column 3, lines 1-53).

Zaccherini fails to teach wherein said transistor gate region being situated over a well and said field oxide region not being situated over said well. However, Erdeljac et al. (Figs.8-11) teach a method to form semiconductor devices including polysilicon resistors and transistors formed on a substrate (10, 12, 18), wherein said substrate (10, 12, 18) includes a well region (18) and wherein said method includes forming resistors (32, 34, 56) over a field oxide region (20); forming a transistor region (44), wherein said transistor region (44) and said resistors (32, 34, 56) are formed in a doped epitaxial layer (12); and further teach forming gate electrode regions (50) over a well (18), wherein said field oxide region (20) having said resistors (32, 34, 56) formed therein is located away from said well (18) (column 5, line 10 – column 6, line 21). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Zaccherini and Erdeljac et al. to enable forming the gate transistors and field oxide regions of Zaccherini on the substrate of Erdeljac et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to

alternative suitable methods of forming the gate electrodes and the field oxide regions of Zaccherini and art recognized suitability for an intended purpose has been recognized to be motivation to combine (MPEP 2144.07), and furthermore, because this would result in an integrated circuit having reduced processing steps (Erdeljac et al. column 4, lines 21 – 45).

The combined teachings of Zaccherini and Erdeljac et al. fail to teach wherein the resistor region of said polycrystalline silicon layer includes an inner portion and an outer portion and further comprises the steps of forming a silicide blocking layer in said inner portion of said resistor region after said step of doping said layer over said transistor gate region and said field oxide region with said second dose of said second dopant; doping said outer portion of said resistor region of said polycrystalline silicon layer with a third dopant so as to form a high-doped region in said resistor region after said step of forming said silicide blocking layer over said inner portion of said layer over said field oxide region, wherein said third dopant has said second conductivity type; and fabricating a contact region over said high-doped region in said outer portion of said resistor region of said polycrystalline silicon layer after said step of doping an outer portion of said layer over said field oxide region, wherein said contact region being electrically connected to said resistor region.

However, Shao et al. (Figs.1-7) in a related method to form implanted regions teach forming a layer (16) comprising polycrystalline silicon over a transistor gate region and a field oxide region (12); doping the field oxide region (12) having said polycrystalline silicon therein with a dopant of a first conductivity type, thus forming a

resistor region (38); forming a transistor gate region (40) by patterning the polysilicon layer (16); and, in a separate doping step, forming a blocking oxide layer (60) in an inner portion of said resistor; doping an outer portion of said resistor region (38) of said polycrystalline silicon layer (16) after forming said blocking layer (60) with a dopant of said first conductivity type so as to form a high-doped region (72, 74) in said resistor region; and fabricating a contact region (column 8, lines 9 – 20) over said high-doped region (72, 74) in said resistor region (38) of said polycrystalline silicon layer (16) after said doping, said contact region (72, 74) being electrically connected to said resistor region (38) (column 4, line 20 – column 8, line 42).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Zaccherini and Erdeljac et al. with the teachings of Shao et al. to enable forming high doping areas and electrical contacts in the high resistivity resistor of Zaccherini and Erdeljac et al., as taught by Shao et al., since this would result in the formation of electrical points of contact (Shao et al., column 8, lines 9 – 10) and eliminates the use of contact mask implant (Shao et al., column 8, lines 5 – 7).

The combined teachings of Zaccherini, Erdeljac et al. and Shao et al. fail to each wherein said first dose of said first dopant is higher than said second dose of said second dopant such that said transistor gate electrical properties are unaffected by said second dose of said second dopant. However, the same materials are treated the same way and therefore the same result would be obtained. Therefore, the

combination of Zaccherini, Erdeljac et al. and Shao et al. teach upon the claimed limitation.

Furthermore, the resistor layer in the combined teachings of Zaccherini, Erdeljac et al. and Shao et al. has to be formed prior to forming the blocking layer, the doping with the third dopant, and the forming of the contact regions, it would have been obvious to one of ordinary skill in the art at the time the invention was made that Zaccherini in view of Erdeljac et al. and Shao et al. teach upon the claimed limitation.

In reference to claims 3-12, 15 and 17-23, the combined teachings of Zaccherini, Erdeljac et al. and Shao et al. teach wherein said layer comprises polysilicon (Zaccherini, column 3, lines 1 – 6); wherein said transistor region is an NFET or an PFET (Shao et al., column 5, lines 7 – 21); wherein said field oxide region comprises silicon oxide (Zaccherini, column 2, lines 53 – 61); wherein the first dopant is an N-type dopant comprising phosphorous at a dose of approximately $1x10^{15}$ to $1x10^{16}$ atoms per square centimeter (Zaccherini, column 3, lines 23 – 32); wherein the second dopant is a P-type dopant comprising boron at a dose of approximately $1.0x10^{12}$ to $1.0x10^{15}$ atoms per square centimeter (Zaccherini, column 3, lines 44 – 53); wherein said doping barrier comprises a photoresist (Zaccherini, Fig.4); wherein the polycrystalline silicon layer includes a gate region (4) (Zaccherini, column 2, lines 46 – 60); and wherein said contact region comprises a silicide (Shao et al., column 8, lines 8 – 20).

The combined teachings of Zaccherini, Erdeljac et al. and Shao et al. fail to expressly teach wherein said first dopant is doped at a dose of approximately 6.5×10^{15} atoms per square centimeter; and wherein said second dopant is doped at a dose of 1.0×10^{15}

atoms per square centimeter. However, in the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. MPEP 2144.05. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the disclosed dopant concentration disclosed in the combined teachings of Zaccherini, Erdeljac et al. and Shao et al. to arrive at the claimed invention.

(10) Response to Argument

Appellant's arguments filed 02/13/2006 have been fully considered but they are not persuasive.

Appellant argues, "...Zaccherini does not teach, disclose, or suggest sequentially doping a layer over a transistor gate region with a first dose of a first dopant having a first conductivity type, doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity type, forming a silicide blocking layer over the layer over the field oxide region, doping an outer portion of the layer over the field oxide region with a third dopant having the second conductivity type, and fabricating a contact region comprising a silicide over a high-doped region of the outer portion of the layer over the field oxide region, where the first dose of the first dopant is higher than the second dose of the second dopant such that transistor gate electrical properties are unaffected by the second dose of the second dopant, where the transistor gate region is situated over a well and the field oxide region is not situated over the well, and where the field oxide region and the well are situated in a substrate...".

In response to this argument, although Zaccherini was relied upon the teachings of "suggest sequentially doping a layer over a transistor gate region with a first dose of a first dopant having a first conductivity type, doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity type" as argued by the Appellant, Zaccherini was not relied upon the teachings of "forming a silicide blocking layer over the layer over the field oxide region, doping an outer portion of the layer over the field oxide region with a third dopant having the second conductivity type, and fabricating a contact region comprising a silicide over a high-doped region of the outer portion of the layer over the field oxide region" as argued by the appellant.

Furthermore, Zaccherini dopes the same material with the same first and second dopant at doping dosages that overlap those claimed in the invention. Therefore since the same materials are treated the same way, the same result would be obtained.

Also, Appellant argues, "...Zaccherini fails to teach, disclose, or suggest forming a layer over a transistor gate region, which is situated over a well in a substrate, and forming the layer over a field oxide region, which is situated in the substrate but not situated over the well, as specified in independent claim 1...". In response to this argument, Zaccherini was not relied upon the argued limitation. In response to appellant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Furtherstill, Appellants argues, "...Erdeljac does not teach, disclose, or suggest sequentially doping a layer over a transistor gate region with a first dose of a first dopant having a first conductivity type, doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity type, forming a silicide blocking layer over the layer over the field oxide region, doping an outer portion of the layer over the field oxide region with a third dopant having the second conductivity type, and fabricating a contact region comprising a silicide over a high-doped region of the outer portion of the layer over the field oxide region, where the first dose of the first dopant is higher than the second dose of the second dopant such that transistor gate electrical properties are unaffected by the second dose of the second dopant, where the transistor gate region is situated over a well and the field oxide region is not situated over the well, and where the field oxide region and the well are situated in a substrate...". In response to this argument, Erdeljac et al. was not relied upon the claimed limitations. In response to appellant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Still, Appellant argues, "...Shao does not teach, disclose, or suggest sequentially doping a layer over a transistor gate region with a first dose of a first dopant having a first conductivity type, doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity

type...where the first dose of the first dopant is higher than the second dose of the second dopant such that transistor gate electrical properties are unaffected by the second dose of the second dopant, where the transistor gate region is situated over a well and the field oxide region is not situated over the well, and where the field oxide region and the well are situated in a substrate...". In response to this argument, Shao et al. was not relied upon the argued limitations. In response to appellant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Appellant argues, "...the resulting structure in Erdeljac...is substantially different than the structure disclosed in Zaccherini...". In response to this argument, although the final structure of Zaccherini is different than that of Erdeljac et al., the combination is proper because the purpose of relying on Erdeljac et al. was to show that transistor regions can be formed in different areas of conductivity. Also, the additional teachings of Zaccherini and Erdeljac et al. pointed to by Applicants do not negate those relied on.

Appellant argues, particular sequence of step specified in independent claims is not disclosed, taught, or suggested in Zaccherini, Erdeljac, and Shao, either singly or in any combination thereof...". In response to appellant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so

found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Zaccherini teaches forming a resistor region having the claimed sequence used to form the resistor and the transistor region, but fails to teach forming the transistor region on a well region, wherein the field oxide region is located outside said well region. The purpose of adding Erdeljac et al. was to show that transistor regions could be formed in different areas of conductivity, as mentioned hereinabove. Still, the combination of Zaccherini and Erdeljac et al. fail to teach the claimed sequence of steps to form the contacts. The purpose of adding the teachings of Shao et al. was to include said teachings. And, as mentioned above, the resistor layer in the combined teachings of Zaccherini, Erdeljac et al. and Shao et al. has to be formed prior to forming the blocking layer, the doping with the third dopant, and the forming of the contact regions, it would have been obvious to one of ordinary skill in the art at the time the invention was made that Zaccherini in view of Erdeljac et al. and Shao et al. teach upon the claimed limitation. Therefore, the rejection in view of Zaccherini, Erdeljac et al. and Shao et al. is proper.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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